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| Department of Electronics  EL-401 Final Year Design Project  **Proposal for the Final Year Design Project** | | | |
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| **Title** | **Implementing AES Encryption and Decryption on a RISC-V Processor** |

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| Domain 1  **Embedded Systems** | Domain 2  **Network Security** | Domain 3  **Data Security** | Domain 4  **Processor Design** | Domain 5  **Cryptography** |

1. **Nature of Project**

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| New Project OR  Extension of Existing Project | Industrial Collaboration | Funded |
| Other Department Collaboration  (If yes) Department Name: **Telecommunication** | Other Academic Institution Collaboration  (If yes) Institution Name\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ | |

1. **Brief Outline**

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| This project aims to develop a high-performance implementation of the Advanced Encryption Standard (AES) algorithm for encryption and decryption on the RISC-V architecture. The goal is to create a fast, efficient, and secure AES implementation on RISC-V architecture build on FPGA.  AES stands for Advanced Encryption Standard and is developed in 2001 before AES the (Data Encryption Standard) DES was used which is bit-Oriented and has a key size of 56 bits and include 16 round but comparing the security factor AES is far more secure the DES.The following Numbers shows the time taken to get the plain text from an encrypted text using Brutal Force Attack.  **56 bit KEY DES Algorithm** Using 56 bit the total combination of key is   wps ≈ 72,000,000,000,000,000Using a computer capable of 1 million key per second it will require approximately 60 days. **[ 1]**  **128 bit KEY AES Algorithm** Using 128 bit the total combination of key is   C:/Users/PC/AppData/Local/Temp/wps.PGJNVqwps Using a computer capable of 1 million key per second it will require approximately 1 Billion Year to generate all possible keys. **[ 2]**  **192/256 bit KEY AES Algorithm** Using 192/256 bit the total combination of key is   C:/Users/PC/AppData/Local/Temp/wps.bLMLlvwps  **or** C:/Users/PC/AppData/Local/Temp/wps.dBVWMuwpsIt will require almost an infinite time to access or generate all the possible keys. **[2]**  AES is far more secure then DES that’s why its application and usage widely expanded across the sector where secure Data transmission is needed. Such as   * Wireless security * Data Storage * Secure Banking * Industrial data security * Communication Pathway * Iot Devices data Transmission   As RISC-V adoption grows in various sectors, including IoT devices, embedded systems, and data centers, there's an increasing need for robust security solutions optimized for this architecture. While AES implementations exist for other architectures, there's a gap in highly optimized versions for RISC-V. This project addresses that gap by providing a tailored AES solution for RISC-V platforms.  Current AES implementations may not fully leverage the RISC-V architecture's capabilities, resulting in sub optimal performance for encryption and decryption operations. This can lead to increased power consumption, reduced throughput, and potential bottlenecks in data processing for RISC-V based system |

1. **Objectives**

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| The project's main contribution is developing a fast AES algorithm implementation that processes data efficiently on RISC-V architecture. The main objectives of the Project are:   1. Design and implement a high-performance AES accelerator 2. Minimize clock cycles required for encryption and decryption 3. Reduce memory footprint and power consumption 4. Ensure Secure and Efficient data transmission in real world.   By achieving these goals, the project will provide a crucial security component for RISC-V based systems, enabling faster and more efficient data protection across a wide range of applications. |

1. **Scope**

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| The project covers the implementation of AES on a RISC-V processor, including optimization for performance and security, testing in secure communication scenarios, and validation against common cryptographic attacks.  The whole FYDP session over the next 2 semesters will comprise of A functional AES encryption and decryption module on a RISC-V processor.Report on the implementation, testing, and performance of the project, documentation for the AES module.  Throughout this project, the following chronology is established:   * Completion of design phase * Integration of AES algorithm and and design on a FPGA * Completion and certification of testing phase.   The constraints and limitations involves project completion within the due date, budget restrictions and availability of lab resources.  The future applications for AES encryption module include but are not limited to SMS encryption for mobile communication on Android message Application[3] only, A Secure Web-Based Android Chat Application[4], AES is one of the two common methods used in IoT devices[5].  There are some scope exclusions like implementation of other encryption standards like DES and implementation on non-RISC-V architectures. |

1. **Proposed Methodology**

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| C:\Users\PC\Desktop\fyd\Proposed Methodolgy (1).pngProposed Methodolgy (1)  Figure 1. Proposed Methodology   1. **Development of RISC-V core**   **Designing a RISC-V core on Quartus Prime for implementing the AES algorithm using Verilog or System Verilog. Connect a memory design to our processor to store the program data and the data to be encrypted or decrypted Peripheral devices for the data input and output we would use a USB to give data input to encrypt and store the encrypt data in USB as well as shown in Figure 1.**   1. **Algorithm Implementation on RISC-V**   **AES Encryption Module on RISC-V:**   * + Implement the AES algorithm tailored to the RISC-V instruction set.   + Include key expansion, substitution, permutation, and mixing operations.   **AES Decryption Module on RISC-V:**   * + Implement the reverse AES process to decrypt cipher text back to plain text, ensuring accuracy with the decryption key.   Four different stages are used, one of permutation and three of substitution: [ 6] As shown in Figure 2.   1. **Substitute bytes:** Uses an S-box to perform a byte-by-byte substitution of the block. 2. **Shift Rows:** A simple permutation. 3. **Mix-columns:** A substitution that makes use of arithmetic over GF(28). 4. **Add Round Key:** A simple bit wise XOR of the current block with a portion of the expanded key   AES Working method  Figure 2 Basic AES encryption and decryption process. [ 7]   1. **Integration**  * Integrate AES Encryption and Decryption Module within the RISC-V core Designed System as shown in Figure 1. * Test encryption and decryption using various data sets on the RISC-V processor to verify correctness and performance.  1. **Validation and Throughput**  * Measuring the throughput by providing different data length input and measuring the time taken by the system to encrypt it. * Validate the system in real-world scenarios, such as secure data transmission or storage, to ensure robustness. |

1. **Resources Involved**

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| **Hardware:**  **FPGA board to develop a design including RISC-V core**, memory modules, programming tools, and peripherals.  **Software:**  Quartus or Vivado, Modelsim , Questasim, RISC-V tool chain, simulation tools, and security testing software. |

1. **Description of Industrial Support (If any)**

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| No industrial support is involved in this project. |

1. **SDGs (If Applicable)**

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| No Poverty | Zero Hunger |
| Good Health and Well-Being | Quality Education |
| Gender Equality | Clean water and Sanitation |
| Affordable and Clean Energy | Decent Work and Economic growth |
| Industry, Innovations and Infrastructure | Reduced Inequalities |
| Sustainable Cities and Communities | Responsible Consumption and Production |
| Climate action | Life Below Water |
| Life on Land | Peace, Justice and Strong Institutions |
| Partnerships |  |

1. **Gantt Chart**

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| Year | 2024 to 2025 | | | | | | | | | |
| Months | AUG | SEP | OCT | NOV | DEC | JAN | FEB | MAR | APR | MAY | |
| Requirement Analysis & Literature Review | x | x | x | x | x | x | x |  |  |  | |
| RISC-V core Development |  | x | x | x |  |  |  |  |  |  | |
| AES Algorithm |  |  | x | x | - | x |  |  |  |  | |
| Integration |  |  |  |  | - | x | x | x |  |  | |
| Validation & Throughput |  |  |  |  | - |  | x | x | x |  | |
| Documentation & Report |  |  | x | x | - | x | x | x | x | x | |

1. **Details of Project Team**
2. **Students**

|  |  |  |  |
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| No. | Name | Seat No. | Signature (s) |
| 1 | Muhammad Tariq Waseem | El - 21056 |  |
| 2 | Mirza Musab Baig | El - 21057 |  |
| 3 | Rameez Nawaz | El - 21061 |  |
| 4 | Anas Uddin | El - 21067 |  |

1. **Supervisors / Advisors**

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| --- | --- | --- | --- | --- |
|  | Name | Designation & Department | Address & Contact | Signature(s) |
| Supervisor | **Hafsa Amanullah** | Lecturer of Electronics Department | [hafsa@cloud.neduet.edu.pk](mailto:hafsa@cloud.neduet.edu.pk) +92 301 2430439 |  |
| Co-Supervisor  (If any) | **Faheem-ul-Haq** | Assistant Professor of Telecommunications | [Mfahim@cloud.neduet.edu.pk](mailto:Mfahim@cloud.neduet.edu.pk) +92 315 0224430 |  |
| Industrial Advisor (If any) | - | - | - |  |

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| **For Office Use Only** | | |
| Project Serial No.: \_\_\_\_\_\_\_\_\_\_  Dated: \_\_\_\_\_\_\_\_\_\_\_\_\_\_ | Signature  Convener Steering Committee | Signature  FYP Coordinator |

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| Proposal Approved | | Not Approved | Returned for Clarification / Modification |
| Comments:  (if any) |  | | |

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|  | (Signature of Chairperson) |
| Date: |  |

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